Notice of Allowability	Application No.	Applicant(s)	
	09/539,463	SELVIDGE ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3-31-2005*.

2. ☒ The allowed claim(s) is/are *1-16*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☒ to Paper No./Mail Date *2-20-2004*.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 6-22-2004.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/28/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

And

REASONS FOR ALLOWANCE

1. **Claims 1-16** are **allowed.**

2. The Examiner withdraws the 35 U.S.C. 112 rejections in view of Applicant's arguments and amended claim language.

Drawings

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the current drawings are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Examiner's Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance:

The following limitations, in combination with other limitations are not anticipated nor made obvious, by the prior art.

"Transmitting or receiving over a serial connection" in combination with *"Transmitting or receiving a framing sequence serially"* and in further combination with *"wherein each bit in said framing sequence and said data packet is transmitted at a single level over two transmit/receive clock periods"*. The Examiner notes further that the Applicant argued in the (3-31-2005 response on page 6), *"Thus, in contrast to claim 1, the FM encoding scheme in Barr uses at least two levels for each bit. Barr later refers to a separate digital audio interface protocol at col. 3 lns. 62-62, stating that 192 bits of data are transmitted as a group with 256 transmit clocks. This means that the digital audio interface protocol does not transmit a bit over two clock cycles as claimed."*

The Examiner further notes that in **U.S. Patents 5,960,191 and 5,943,490** is disclosed, in **Figure 8** and **Col. 11 lines 51-58,** *"The pulse emitted on External Signal **146** may have a width of one, **two**, three, or four clocks depending on whether the two Design Signals **140** and **142** had values of 00, 01, 10 or 11 when a signal transition occurred. Asynchronous Clock Signal **144** must however, be sufficiently fast that **five** clock cycles **always** elapse between successive edges of Design Signals **140** and **142** to ensure that information is not lost"* and in **Col. 2 lines 47-51** discloses, *"These prior art emulation systems, however, alter or re-synthesize clock paths in an attempt to maintain correct circuit behavior. This alteration or re-synthesis process works predictably for synchronous designs. However, altering or re-synthesizing the clock paths in an asynchronous design can lead to inaccurate or misleading emulation results."* It is noted by the Examiner that this passage from **U.S. Patent 5,960,191** is directed to the Applicant's **Col. 2 lines 39-40,** *"Other prior art hardware emulation systems such as those available from Virtual Machine Works (now IKOS),"* The Examiner notes that the disclosed passage from the cited

reference does not disclose the use of *"each bit in said framing sequence and said data packet is transmitted/received at a single level over two transmit/receive clock periods"*, in fact the **5,960,191** reference teaches away from using the claimed methodology and in fact ***requires*** the use of *five* clock periods **(Col. 11 line 56)**. The Examiner further notes that neither of the cited references teach each bit being transmitted/received using a *single level* for *each bit of the framing sequence* being sent using *two transmit/receive clock periods* wherein the **5,960,191** reference teaches encoding *multiple bits* **(*see Figure 8 item 146 the data encoded during the clock periods is a group of two bits and not a single bit as expressly claimed by the Applicant.*)**

In view of the expressly claimed limitations in Applicant's instant amendments and in further view of Applicant's arguments, the Examiner withdraws all previously applied prior art rejections and allows Independent **Claims 1, 2, 5 and 11.**

4.1 Dependent **Claims 3, 4, 6-10 and 12-16** are allowed as they depend upon an allowed base claim.

4.2 Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,836,757 discloses serial test ports in emulation systems **(Abstract).**

U.S. Patent 5,761,484 discloses a *"softwire"* compiler in an FPGA emulation system **(Abstract).**

U.S. Patent 5,596,742 discloses a *"softwire"* compiler in an FPGA emulation system **(Abstract).**

"Tiers: Topology IndependEnt Pipelined Routing and Scheduling for VirtualWire Compilation" discloses, a *"Virtual Wire"* technology for routing in an FPGA based design.

5.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P Picard can be reached on (571)272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER